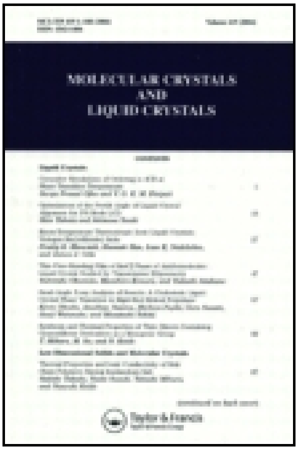

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Fabrication of Organic Thin-Film Transistors Based on High Dielectric Nanocomposite Insulators

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Organic thin-film-transistors (OTFTs) with solution-processed high dielectric gate insulators were fabricated. The gate insulators were made of high dielectric TiO_2 nanoparticles dispersed uniformly in a polymer matrix of nylon 6 which is known to align liquid crystal molecules. It was found that the nanocomposite insulator in a pentacene-based OTFT reduces the operating voltage but it produces substantial current leakage. A buffer layer of polyvinylphenol on the top of the nanocomposite layer was found to block the leakage current and to increase significantly the carrier mobility as well as the current on-off ratio.

Keywords: leakage current; nanocomposite; OTFTs; operating voltage; polymer buffer layer

INTRODUCTION

Recently, organic thin-film-transistors (OTFTs) have received considerable attention because of their wide applications in displays, sensors, and logic circuits [1–3]. Compared with conventional

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inorganic TFTs, the OTFTs show inherent advantages of low cost, compatibility with flexible substrates, and large area processing. Moreover, the performances of pentacene-based OTFTs have reached to a similar level of amorphous silicon TFTs [4]. However, the operating voltage of the OTFT is often too high to be used for practical applications. The reduction of the operating voltage has been reported using high-k (k: dielectric constant) metal oxides for gate insulators [5].

Conventional high-k metal oxides have been deposited either by the sputtering [5] or the anodization process [6]. However, the sputtering or anodization process would not be compatible with the OTFT fabrication on flexible substrates over large area due to the high temperature process. In addition, the patterning process through etching is not desirable for organic semiconductor materials. Thus, it is very important to develop solution-processable high-k dielectric materials for applications in flexible electronics. Since the solution-process such as spin-coating, casting, and printing can be done at a low temperature, it is suitable for fabricating the OTFT when combined with low-cost patterning techniques. Among the soluble dielectrics prepared at low-temperatures, the nanocomposite of high-k nanoparticles in a polymer has been known to exhibit the largest value of k [7].

However, a typical nanocomposite film of TiO_2 suffers from a large leakage current [8] and usually contains highly hydrophilic surfaces that are less compatible with the growth of organic semiconductor materials such as pentacene [9]. Considering that ultra-thin polymer buffer layers have been used for high-k metal oxides to reduce the leakage current and to modify the surface of the oxide film more hydrophobic [5,6], one way of circumventing the above drawbacks is to stack the polymer layer on the nanocomposite film.

In this work, we have fabricated OTFTs with solution-processable gate insulators. The gate insulator is made of high-k TiO_2 nanoparticles, dispersed uniformly in a polymer matrix of nylon 6, to reduce the operating voltage and a polymer buffer layer of polyvinylphenol (PVP) to reduce the leakage current. Using a thin PVP buffer layer prepared on the nanocomposite layer, a reduced leakage current, an enhanced carrier mobility, and a high current on-off ratio are obtained.

EXPERIMENTAL

Figure 1 shows a schematic diagram of our OTFT. The Al layer was deposited on a glass substrate as a gate electrode by thermal evaporation. The gate insulator consists of two layers, a nanocomposite layer and a buffer layer. In our study, TiO_2 nanoparticles with the high dielectric constant ($k =$ **42 at 1 kHz**) were used [10]. **It is noted that**

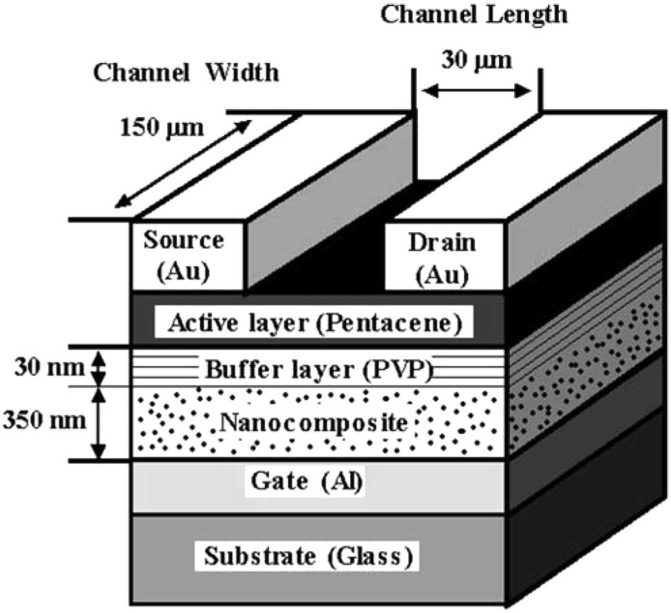


FIGURE 1 The schematic diagram of OTFT.

fluctuations of the dielectric properties of a polymer film are known to be intrinsically high at high frequencies, so that a relatively low frequency of 1 kHz is typically used to determine the dielectric constant of a polymeric insulator layer [11].

Nylon 6 was selected as a polymer matrix in which nanoparticles were uniformly dispersed. Note that nylon 6 ($k = \mathbf{4}$ **at 1 kHz**) [12] is known to have the capability of aligning liquid crystal molecules so that the structural order of buffer polymers and/or semiconductor molecules may be induced [13]. Such induced structural order is expected to play an important role in improving the carrier mobility of OTFTs.

Nylon 6 was first dissolved in 222-trichloroethanol at the concentration of 2 wt.% to disperse uniformly nanoparticles. Subsequently, the TiO_2 colloid (15 wt.% in methanol) was introduced into the nylon 6 solution. The volume ratio of the TiO_2 nanoparticles to nylon 6 in the composite solution was about 30:70. No apparent precipitation was found even after several weeks in the composite solution. For producing conformal nanocomposite films, certain amounts of the solvents in the composite solution (about 33 wt.% of the composite solution) were evaporated in a vacuum oven to adjust the viscosity which is closely related to the morphology of the spin-coated films [14]. Spin-coated nanocomposite layers were soft baked at 80°C for 60 min, then hard baked at 140°C for 90 min in a vacuum oven. The thickness of the nanocomposite gate insulator was about 350 nm. The dielectric constant of the nanocomposite layer, measured by an impedance analyzer (HP4192A), was about 14 at 1 kHz.

PVP ($k = 4$) was selected for the polymer buffer layer because it is known to produce the high mobility for pentacene based OTFTs [8,15]. A solution of PVP in isopropylalcohol at the concentration of 1 wt.% was spin coated onto the top of the nanocomposite layer to form a buffer layer. Note that the polymer matrix of nylon 6 is chemically stable against the solution of PVP. The thickness of the PVP layer was about 30 nm which is only a tenth of that of the nanocomposite layer. The effective total dielectric constant of the two layers, the nanocomposite and the PVP, was measured as about 11 at 1 kHz.

As an active layer, pentacene was thermally evaporated on the gate insulator at the deposition rate of 0.5 Å/sec under a pressure of about 10^{-6} Torr. The thickness of the pentacene layer was 60 nm. During the evaporation, the substrates were held at room temperature. Au was thermally deposited on the top of the pentacene film to prepare the source electrode and the drain electrode through a shadow mask. The length and the width of the channel were 30 µm and 150 µm, respectively. The electrical characteristics were measured using the Keithley 238 source-measurement unit and ELECS Semiconductor Test and Analyzer under the ambient pressure at room temperature.

RESULTS AND DISCUSSION

The dispersion of TiO_2 nanoparticles in the nylon 6 polymer matrix was investigated by the scanning electron microscope (SEM). Figures 2(a) and 2(b) show the SEM image in the substrate plane and that of the cross-section of the nanocomposite layer, respectively. It is clear that the TiO_2nanoparticles, represented by white spots in Figure 2, were uniformly dispersed over the whole area. This suggests that solution-processed nanocomposites are promising for producing high-k gate dielectrics.

The surface morphologies of the gate dielectrics and the grain sizes of the pentacene layers were shown in Figure 3. The AFM images of the nanocomposite layer and the pentacene layer deposited on the nanocomposite layer were shown in Figures 3(a) and 3(c). A large morphological difference between the nanocomposite layer and the pentacene layer was observed. In contrast, only a small difference between the nanocomposite with the PVP buffer layer and the pentacene film

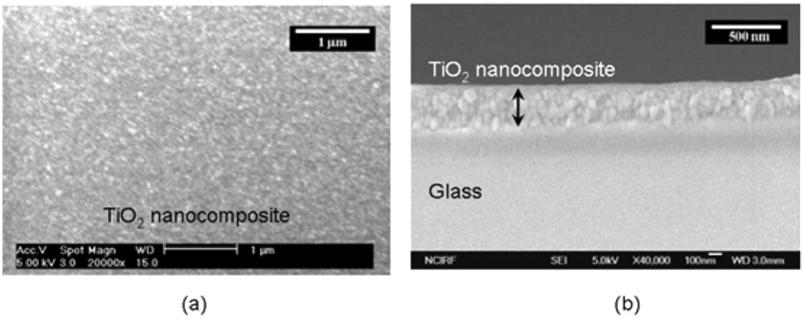


FIGURE 2 The SEM images of the nanocomposite film: (a) the surface of the nanocomposite film and (b) the cross-section of the nanocomposite film.

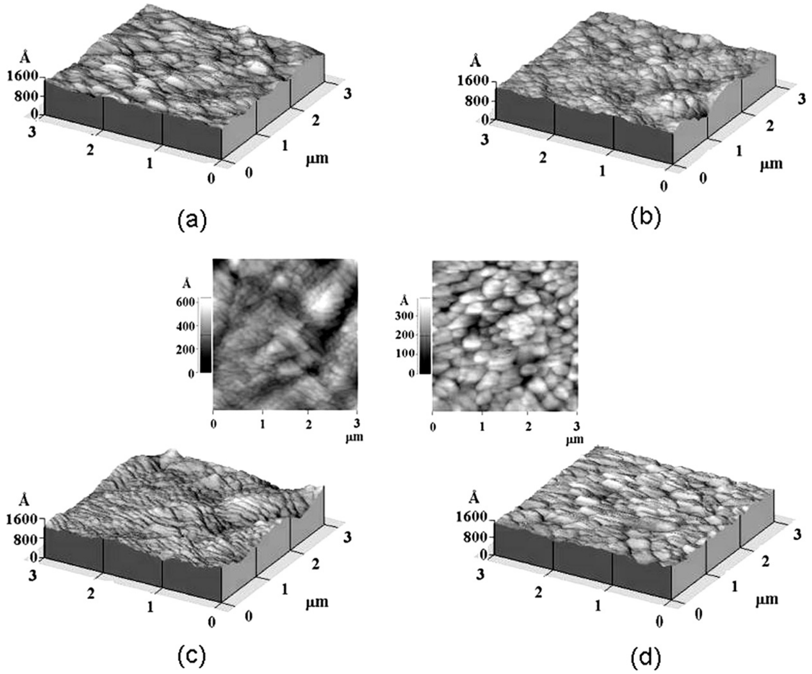
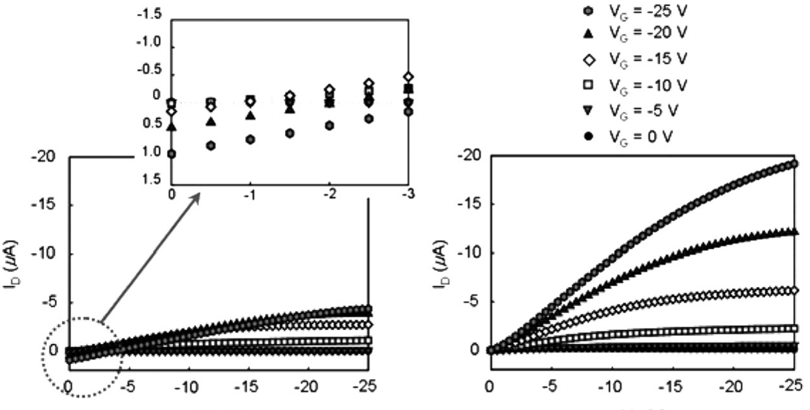


FIGURE 3 The AFM images of the insulator layer and the pentacene film deposited on the insulator layer: (a) a nanocomposite layer, (b) a nanocomposite with the buffer layer of PVP, (c) the pentacene film deposited on the nanocomposite layer, and (d) the pentacene film deposited on the nanocomposite with the buffer layer of PVP.

was seen in Figures 3(b) and 3(d). An interesting point is that the pentacene layer on the nanocomposite with the PVP layer is smoother than that on the nanocomposite layer only although the root-mean-square value of the roughness remains same as about 7 nm in both cases. Moreover, the average grain size in the pentacene film deposited on the nanocomposite with the PVP buffer layer is significantly larger than that in the pentacene film deposited on the nanocomposite layer only. Since a large grain size generally produces a significant increase in the mobility, the introduction of the PVP buffer layer is important to increase the mobility of OTFTs.

Figures 4(a) and 4(b) show the plots of the drain-source current (I_D) versus the drain-source voltage (V_D) at different gate voltages (V_G) for the OTFT with the nanocomposite only and the OTFT with both the nanocomposite and the buffer layer, respectively. The nonzero current at the drain bias of 0 V with increasing the gate voltage results from the current leakage through the gate dielectric layer between the source/drain electrode and the gate electrode [16]. It is clear that the use of the buffer layer decreases the leakage current by at least two orders of the magnitude.

Figures 5(a) and 5(b) show the characteristic plots of $I_D{}^{1/2}$ versus V_G for the OTFT with the nanocomposite only and the OTFT with both



(a) (b)

FIGURE 4 I_D vs V_D output curves: (a) the OTFT with the nanocomposite only and (b) the OTFT with both the nanocomposite and the buffer layer of PVP. Open hexagons, filled triangles, open diamonds, filled squares, open triangles, and filled circles represent the applied gate voltages of -25 V, -20 V, -15 V, -10 V, -5 V, and 0 V, respectively.

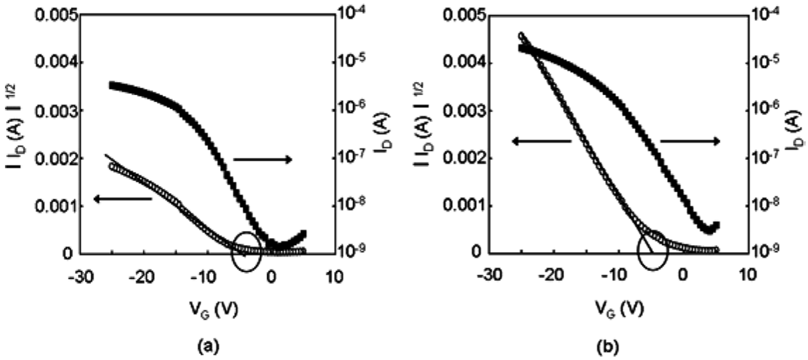


FIGURE 5 ${I_D}^{1/2}$ vs V_G characteristic curves: (a) the OTFT with the nanocomposite only and (b) the OTFT with both the nanocomposite and the buffer layer of PVP. The drain-source voltage at $-20\,\text{V}$ was used to calculate the carrier mobility.

the nanocomposite and the buffer layer at a fixed V_D of $-20\,\text{V}$. The carrier mobility was extracted from Figure 5 using the following equation [17].

$$I_D = \frac{W}{2L} C_i \mu (V_G - V_T)^2,$$

where W and L are the width and the length of the channel, respectively. Here, μ is the carrier mobility, C_i is the insulator capacitance per unit area, V_T and V_G are the threshold voltage and the gate voltage, respectively. Note that the threshold voltages in the two OTFTs are same as about $-5\,\text{V}$. This threshold voltage is about two times lower than threshold voltage of OTFT with single PVP layer of similar thickness. For the OTFT with the nanocomposite only, the carrier mobility was $0.1\,\text{cm}^2/\text{Vs}$ and the current on-off ratio was about 10^3. For the OTFT with both the nanocomposite and the PVP buffer layer, the carrier mobility was $0.7\,\text{cm}^2/\text{Vs}$ and the current on-off ratio was about 10^4. This indicates that the PVP buffer layer plays a critical role in reducing the leakage current for nanocomposite gate insulator, and improving the electrical performances without changing the operating voltage.

CONCLUSION

We demonstrated the OTFTs with solution-processed high dielectric gate insulators. The gate insulator consisted of both the nanocomposite and the PVP buffer layer. High dielectric inorganic nanoparticles, dispersed uniformly in a polymer matrix, reduce the operating voltage of the OTFT but they produce a large leakage current. Thus, for nanocomposite gate insulator, the use of a polymer buffer layer such as the PVP layer is essential to reduce the leakage current and to increase both the carrier mobility and the current on-off ratio. It is concluded that our approach to solution-processed high dielectric insulators would be a powerful method of avoiding complications and being compatible with flexible substrates.

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